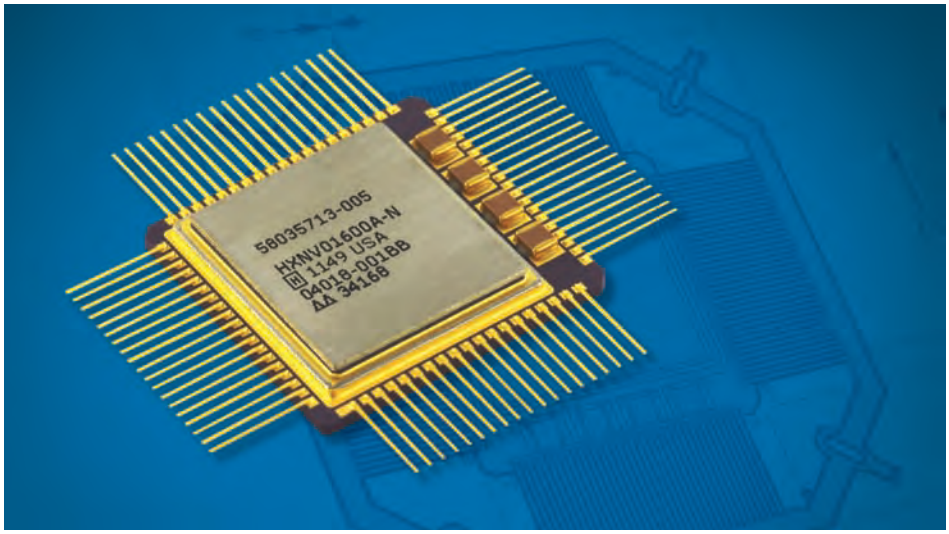
HXNV01600

Honeywell

16 Megabit Non-Volatile Magneto-Resistive RAM

Features

- **Fabricated on S150 Silicon On Insulator (SOI) CMOS Underlayer Technology**
- **150 nm Process**
- **Total Dose Hardness**
  $1x10^6$ rad (Si)
  $3x10^5$ rad (Si)
- **Dose Rate Upset Hardness**
  $1x10^{10}$ rad(Si)/s
- **Dose Rate Survivability**
  $1x10^{12}$ rad(Si)/s
- **Soft Error Rate**
  $\leq 1x10^{-10}$ upsets/bit-day
- **Neutron Hardness**
  $1x10^{14}$ N/cm^2
- **No Latchup**
- **Read Access Time**
  95 ns
- **Read Cycle Time**
  120 ns
- **Write Cycle Time**
  140 ns
- **Robust Write and Read Capability**
- **15 years Data Retention @ 105°C**
- **Synchronous Operation**
- **Address Auto Increment Feature**
- **Single-Bit Error Detection & Correction (ECC)**
- **Core Power Supply**
  3.3V ± 0.3V
- **3.3V or 2.5V CMOS Compatible I/O**
- **Standard Operating Temperature Range is**
  -40°C to +125°C
- **Package: 76 Lead Shielded Ceramic Quad Flat Pack**
- **QML Qualified: SMD 5962-13212**

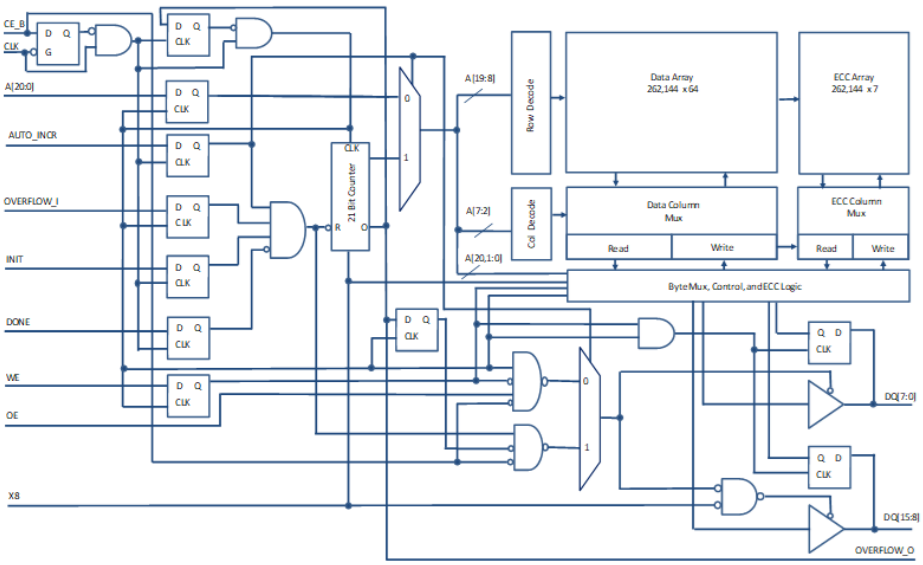


The Honeywell 16 Megabit radiation hardened low power non-volatile Magneto-Resistive Random Access Memory (MRAM) offers high performance and is designed for space and military applications. The part can be configured as either a 2,097,152 word x 8-bit or a 1,048,576 word x 16 bit MRAM through an external pin setting.

The high reliability MRAM is designed for severe space environments and features excellent endurance, integrated Error Correction Coding (ECC) and low-voltage write protection. These features ensure the correct operation of the memory and protection from inadvertent writes.

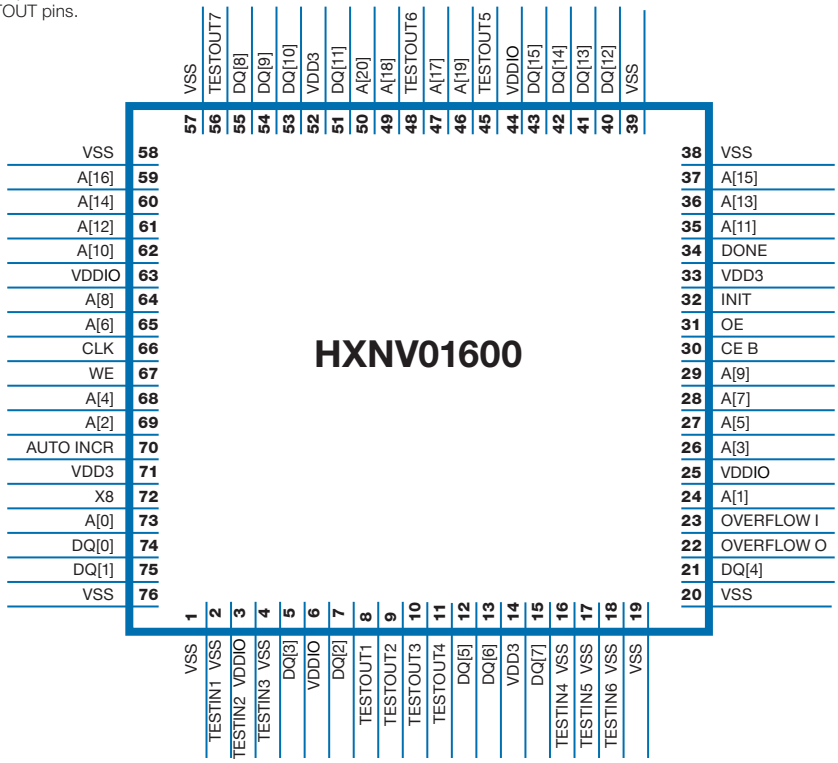
Fabricated with Honeywell's radiation hardened Silicon On Insulator (SOI) technology, the MRAM is designed for use in low-voltage systems operating in radiation environments over a temperature range of -40°C to +125°C with a 3.3 ± 0.3V power supply and 2.5V or 3.3V I/O compatibility.

Functional Block Diagram



Package Pinout

Note: See Signal Description table for proper board connection for TESTIN and TESTOUT pins.



Signal Description

Symbol	Definition
CLK	Rising edge initiates an access of memory. A(20:0), WE, CE B, and DQ(15:0) are latched on the rising edge. High level required for DQ(15:0) outputs to be enabled.
CE B	Active low chip enable. High state at rising edge of CLK disables chip (no memory access and outputs go to high impedance). Low state at rising edge enables an access of the memory.
A(20:0)	Address Word Input. A(20) is MSB, A(0) is LSB. In 16 bit configuration, A(20) is not used and should be tied to VSS.
DQ(15:0)	Data Input/Output Signals. Bi-directional data pins which serve as data outputs during a read operation and as data inputs during a write operation. When in X8 mode, only DQ(7:0) are active and DQ(15:8) pins should be tied to VSS.
WE	Write Enable. Active high write enable. High state at rising edge of CLK initiates a write cycle. Low state at rising edge of CLK initiates a read cycle.
OE	Output Enable. Active high output enable. Low state puts outputs in high impedance state.
X8	Byte Mode Configuration Pin. Active high input. Configures the memory interface as 8 bit when high (DQ(7:0) only active). When low, memory interface is 16 bits(DQ(15:0)). Should be tied directly to VSS or VDDIO depending on desired configuration
AUTO INCR	Auto Increment Mode Enable. Active high input sampled on rising edge of CLK. When high enables internal address counter and read only mode.
OVERFLOW I	Counter Enable Input Pin. Active High Enable for internal counter (when INIT=1,DONE=0). Used to daisy chain devices.
INIT	Active High Interface Pin used to reset internal address counter (when OVERFLOW I=1, DONE=0)
DONE	Active Low Interface Pin used to reset internal address counter (when OVERFLOW I=1, INIT=1).
OVERFLOW O	Internal Overflow Counter Indicator. Active high output signal indicates internal counter has reached last address. Used to daisy chain devices.
VSS	Ground
VDDIO	DC I/O Power Supply Source Input: Nominal 2.5V or 3.3V. VDDIO is the operating voltage for all inputs and output signals.
VDD3	DC Power Source Input: nominal 3.30V
TESTINx	Test input pins not intended for customer use. Connect as defined on Package Pinout diagram to either VSS or VDDIO
TESTOUTx	Test output pins not intended for customer use. Treat as “no connects” to have no connection on the circuit board.

Functional Truth Table

CLK	CE B	WE	AUTO INCR	INIT	DONE	OVERFLOW I	FUNCTION
R	0	0	0	X	X	X	Read Cycle (1)
R	0	1	0	X	X	X	Write Cycle (1)
R	1	X	X	X	X	X	Chip Disable
R	0	X	1	1	0	1	AI Read Cycle (2) (3)
R	X	X	1	0	X	X	Chip Disable (2) (4)
R	X	X	1	X	1	X	Chip Disable (2) (4)
R	X	X	1	X	X	0	Chip Disable (2) (4)

(1) Read and Write occurs at memory location provide by Address Pins at rising edge of CLK
(2) Auto Increment Read Modes
(3) Internal Address Counter Starts with Address = 0x00000 and increments 1 per rising edge of CLK
(4) Internal Counter Reset to Address = 0x000000

Output Driver Truth Table

FUNCTION	CLK	OE	CE B	Data Outputs
Read Cycle	1	1	X	Active
Read Cycle	1	0	X	Hi-Z
Read Cycle	0	X	X	Hi-Z
Write Cycle	X	X	X	Hi-Z
Chip Disable	X	X	X	Hi-Z
Auto Inc Read Cycle	X	X	0	Active
Auto Inc Read Cycle	X	X	1	Hi-Z

Magnetic Memory Technology

The memory element is a magnetic tunnel junction (MTJ) that is non-volatile and composed of a magnetic storage layer structure and a magnetic pinned layer structure separated by an insulating tunnel barrier. During a write cycle, the storage layer is written by the application of two orthogonal currents using row-and-column addressing. The MTJ resistance depends on the magnetic state of the storage layer structure, which uses the pinned layer structure as a reference, and enables signal sensing, amplification, and readback. The memory element resistance is a result of the change in Tunneling Magneto-Resistance (TMR) between the storage and pinned layers that results from the magnetic state of the storage layer.

Error Correction Code (ECC)

Hamming 7-Bit ECC

A 7-bit Hamming ECC is generated for all data written into memory. This code allows for the correction of all single-bit errors per internal 64 bit word. On a read cycle, a data word is read from memory and corrected, if necessary, before being placed on the output data bus. There is no change made to the actual data in the memory cells based on the ECC results. Actual data in memory are changed only upon writing new values.

Radiation Characteristics

Total Ionizing Radiation Dose

The MRAM has a radiation hardness assurance TID level of 300 Krad and 1Mrad(Si), including overdose and accelerated annealing per MIL-STD-883 Method 1019. Total dose hardness is assured by qualification testing with a Co60 source and wafer level X-ray testing during manufacturing.

Soft Error Rate

Special process, cell, circuit and layout design considerations are included in the MRAM to minimize the impact of heavy ion and proton radiation and achieve a very low radiation induced Soft Error Rate (SER). Weibull parameters and other relevant attributes are available upon request to calculate projected upset rate performance for other orbits and environments.

Transient Pulse Ionizing Radiation

Many aspects of product design are addressed to handle the high energy levels associated with the transient dose events. This allows the MRAM to be capable of writing, reading, and retaining stored data during and after exposure to a transient ionizing radiation pulse, up to the specified transient dose rate upset specification.

The MRAM will also meet functional and electrical specifications after exposure to a radiation pulse up to the transient dose rate survivability specification.

Neutron Radiation

SOI CMOS is inherently tolerant of neutron radiation. The MRAM meets functional and timing specifications after exposure to the specified neutron fluence, based on conventional neutron irradiation testing, on unpowered MRAM parts.

Latchup

The MRAM will not latch up due to any of the above radiation exposure conditions when applied under recommended operating conditions. Fabrication with the SOI CMOS substrate material provides oxide isolation between adjacent PMOS and NMOS transistors and eliminates any potential SCR latchup structures.

Radiation-Hardness Ratings (1)

Parameter	Limits	Units
Total Ionizing Dose H-Level	1×10^{6}	Rad(Si)
F-Level	3×10^{5}	
Transient Dose Rate Upset	1×10^{10}	Rad(Si)/s
Transient Dose Rate Survivability	1×10^{12}	Rad(Si)/s
Soft Error Rate (SER) (2)	$\leq 1 \times 10^{-10}$	Upsets/bit-day
Neutron Irradiation (3)	1×10^{14}	N/cm^2

(1) Device will not latch up due to any of the specified radiation exposure conditions.
(2) Geosynchronous Orbit, Solar minimum, 100mils aluminum shielding
(3) 1 MeV equivalent energy, the device is unbiased during test

Magnetic Field Characteristics

Honeywell's MRAM family is designed and manufactured to meet specifications when exposed to magnetic fields up to the ratings defined in the Absolute Maximum table. Exposure to larger magnetic fields may affect functionality.

Recommended Operating Conditions (1)

Specifications listed in datasheet apply when used under the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Description Min	Typ	Max	Units
VDDIO	Positive I/O Supply Voltage (2)	2.25 3.0	2.5 3.3	2.75 3.6	Volts
VDD3	Positive Supply Voltage (2)	3.0	3.3	3.6	Volts
T_C	Case Temperature Voltage	-40	25	125	°C
V_{PIN}	Voltage On Any Pin	-0.3		VDDIO+0.30	Volts
Lifetime (3)	Operational Lifetime			15 @ 105ºC	Years

(1)Voltage referenced to VSS.
(2) There is a 2ms startup time once VDD3 exceeds VDD3(min) and VDDIO exceeds VDDIO(min). See Power Sequencing Section.
(3) Lifetime at +125ºC is 2 years.

Absolute Maximum Ratings (1) (2)

Symbol	Parameter	Ratings Min	Max	Units
VDDIO	Positive I/O Supply Voltage	-0.5	4.6	Volts
VDD3	Positive Supply Voltage	-0.5	4.6	Volts
V_{PIN}	Voltage on Any Pin	-0.5	VDDIO + 0.5	Volts
T_{STORE}	Storage Temperature (5)	-65	150	°C
T_{SOLDER}	Soldering Temperature		220	°C (4)
P_D	Power Dissipation		1.25	W
Θ_{JC}	Thermal Resistance (Junction to Case)		4.0	°C /W
V_{PROT}	Electrostatic Discharge Protection Voltage (3)	2000		V
T_J	Max Junction Temperature		160	°C
H_{field} (6)	Magnetic Field Exposure Write	-----	65	Oe
	Read / Standby	-----	100	Oe
I_{out} (7)	Maximum Output Current	-----	90	mA

(1) Stresses in excess of those listed above may result in immediate permanent damage to the device. These are stress ratings only, and operation at these levels is not implied. Frequent or extended exposure to absolute maximum conditions may affect device reliability.
(2) Voltage referenced to VSS.
(3) Human Body Model.
(4) Maximum soldering temperature can be maintained for no more than 180 seconds over the lifetime of the part.
(5) Storage time above 125°C is limited to 504 hours.
(6) Tested at 25ºC.
(7) Not to exceed 1 second duration.

Capacitance (1) (2)

Symbol	Parameter	Limits Max	Units
C_O	Output Capacitance	15	pF
C_I	Input Capacitance	12	pF

(1) Maximum capacitance is verified as part of initial qualification only.
(2) F = 1MHz

DC Electrical Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
VIL	Low Level Input Voltage		0.3*VDDIO	V	
VIH	High Level Input Voltage	0.7*VDDIO		V	
VOL	Low Level Output Voltage		0.5	V	IOL = 6 mA
VOH	High Level Output Voltage	VDDIO-0.5		V	IOH = -6 mA
IOZ	Output Leakage Current	-100	100	µA	Chip deselected or output disabled
II	Input Leakage Current	-10	10	µA	
IDDSB	Standby Current		18	mA	Sum of VDD3 and VDDIO Standby Current
IDDOP_W	Operating Current WRITE Mode				Sum of VDD3 and VDDIO Operating Current
	1MHz		60	mA	
	7MHz		110	mA	
IDDOP_R	Operating Current READ Mode				Sum of VDD3 and VDDIO Operating Current
	1MHz		40	mA	
	9MHz		90	mA	

Data Endurance (1)

Parameter	Ratings Min	Max	Units
Data Read Endurance	$1x10^{15}$		Cycles
Data Write Endurance	$1x10^{15}$		Cycles

(1) Evaluated as part of qualification.

Data Retention (1) (2)

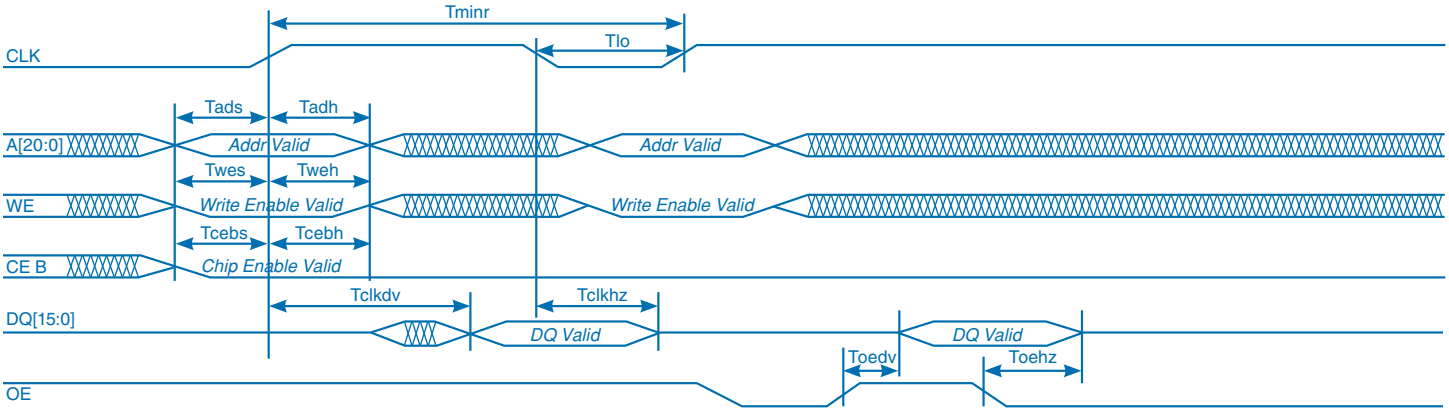
Parameter	Ratings Min	Max	Units
Data Retention	15		years

(1) Evaluated as part of qualification.
(2) Applies with power on or off.

Read Cycle (Random Access Read Using Address Pins)

The non-volatile MRAM is synchronous in operation relative to the rising edge of the CLK signal. With the initiation of a rising CLK signal, the Address and the Write Enable (WE) signals are captured and the read operation begins from the desired memory location. The addressed memory locations are read and compared with the ECC values. Any single bit errors are detected and corrected. If WE was low when captured, the data word is sent to the output drivers. In addition to WE low being captured, Output Enable (OE) must be set to high to enable the DQ output buffers. OE is not captured and may be set high before or after the rising edge of CLK.

Read Cycle AC Timing Characteristics (1)



Name	Description	Min	Max	Units
Tads	Address Setup Time	5	–	ns
Tadh	Address Hold Time	15	–	ns
Twes	WE Setup Time	5	–	ns
Tweh	WE Hold Time	15	–	ns
Tcebs	CE B Setup Time	5	–	ns
Tcebh	CE B Hold Time	15	–	ns
Tclkdv	DQ valid with respect to rising edge of CLK	50	95	ns
Tclkhz	Clock Low to DQ Hi-z	1	15	ns
Toedv	OE access time	–	15	ns
Toehz	OE de-asserted to DQ Hi-z	1	15	ns
Tminr	Read Cycle Time	120	–	ns
Tlo	Clock Low Time	15	–	ns

(1) As measured on Honeywell tester.

Read Cycle (Auto Increment Address Mode)

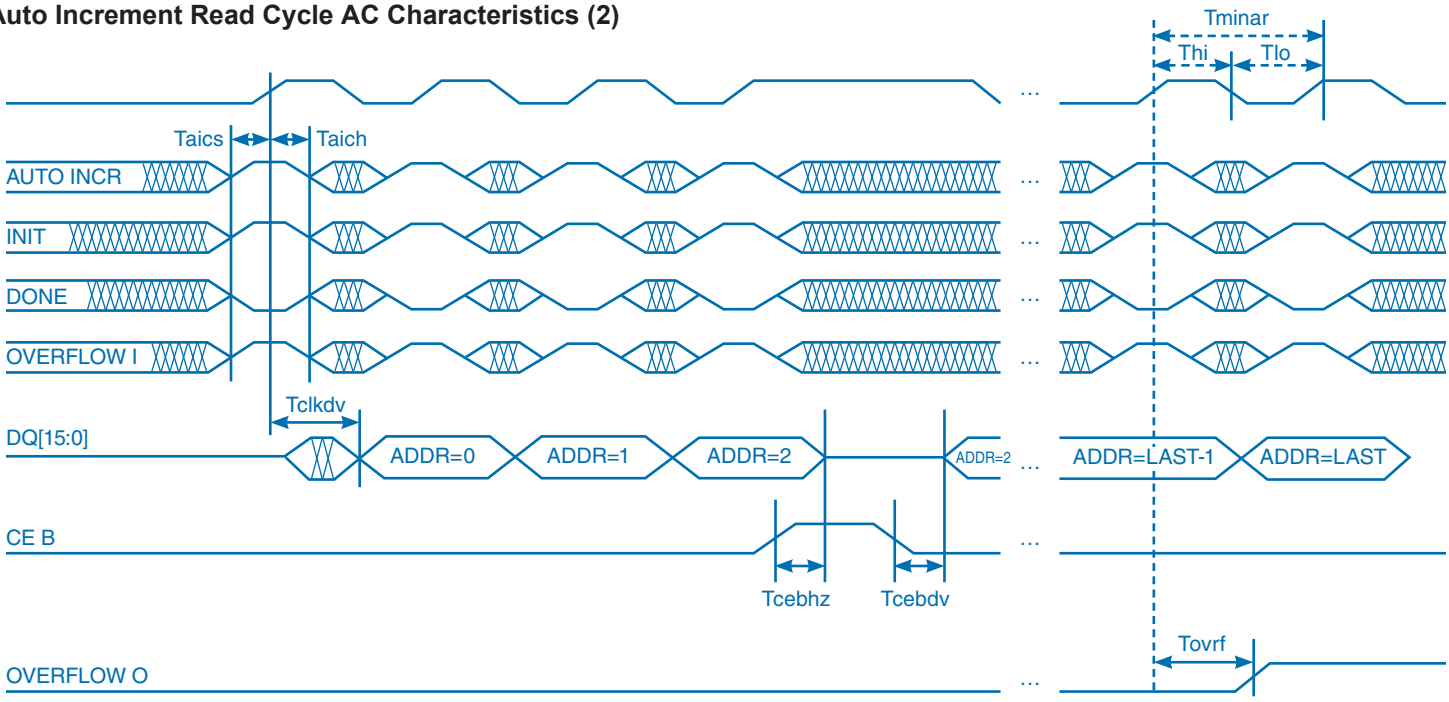
In addition to random memory locations previously described, MRAM can read in an auto incrementing address mode where each rising edge CLK initiates a read from the previous address plus one. When entering this auto increment mode, the first address access always starts at 0. Once the last address is reached, the OVERFLOW O flag is asserted and the chip disables on the next cycle.

With the initiation of a rising CLK signal, the auto increment enable pin (AUTO INCR) and counter enable (INIT, DONE, OVERFLOW I) signals are captured into the device. The auto increment enable pin must be high when captured and the counter enables must be in the correct state (INIT=OVERFLOW I=1, DONE=0) to begin the auto increment read operation. The memory locations are read and compared with the ECC values. Any single bit errors are detected and corrected.

If an auto increment address mode read occurs, the data word is sent to the output drivers. In addition to the auto increment signal being high when captured and counter enables being set correctly, the Output Enable (OE) must be set to high to enable the DQ output buffers.

Following an auto increment overflow condition (OVERFLOW_O = high); a no-op(dummy) clock cycle with CE_B=low and auto_incr=low must be performed to clear the internal overflow register. During this no-op clock cycle the output is high-Z and no read or write operation occurs.

Auto Increment Read Cycle AC Characteristics (2)



Name	Description	Min	Max	Units
Taics	Auto Increment Control Setup Time (1)	5	–	ns
Taich	Auto Increment Control Hold Time (1)	15	–	ns
Tclkdv	DQ valid with respect to rising edge of CLK	50	95	ns
Tovrf	Rising Edge of Clock to OVERFLOW O High	-	10	ns
Tminar	Auto Increment Minimum Read Cycle Time	120	-	ns
Tcebdv	CE B access time	–	15	ns
Tcebhz	CE B de-asserted to DQ Hi-z	1	15	ns
Thi	Clock High Time	15	–	ns
Tlo	Clock Low Time	15	–	ns

(1) Applies to AUTO INCR, INIT, DONE, OVERFLOW I pins.
(2) As measured on Honeywell tester.

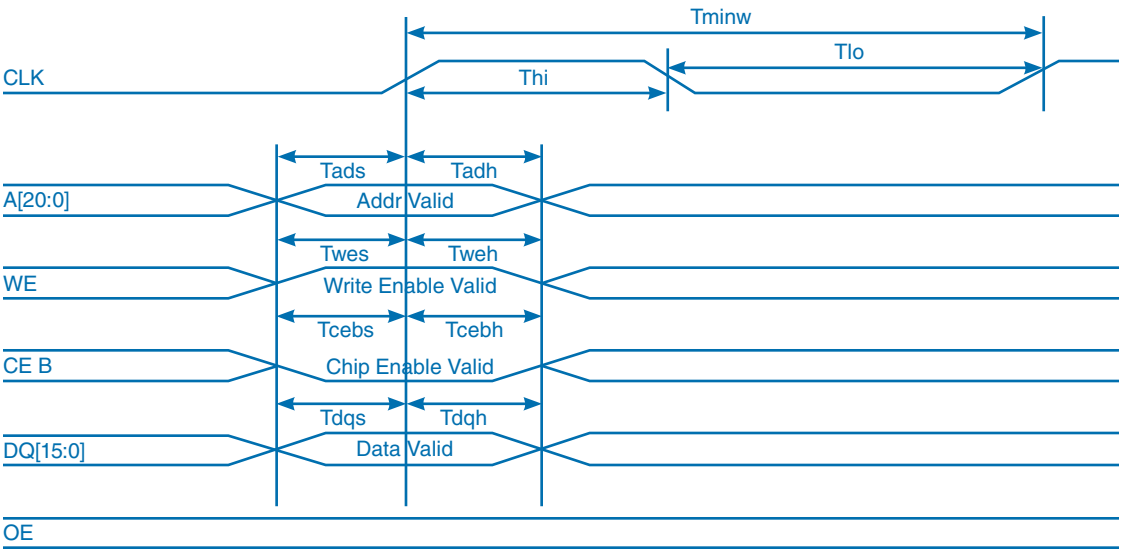
Write Cycle

The MRAM is synchronous in operation relative to the rising edge of the CLK signal. With the initiation of a rising edge CLK signal, the Address and the Write Enable (WE) signal are captured into the device.

The WRITE CYCLE begins by reading the currently addressed value in memory. The current memory data are compared to the data to be written. If the location need to change value, the data are then written.

The bit cell construction of this device does not provide a method of simply writing a “1” or a “0” to match the data. The “write” to a bit can only change its state, thus the need to read the bit locations first. Only the bits which need to “change state” are actually written.

Write Cycle AC Timing Characteristics (1)



Name	Description	Min	Max	Units
Tads	Address Setup Time	5	–	ns
Tadh	Address Hold Time	15	–	ns
Twes	WE Setup Time	5	–	ns
Tweh	WE Hold Time	15	–	ns
Tcebs	CE B Setup Time	5	–	ns
Tcebh	CE B Hold Time	15	–	ns
Tdqs	Data Setup Time	5	–	ns
Tdqh	Data Hold Time	15	–	ns
Tminw	Write Cycle Time	140	–	ns
Thi	Clock High Time	15	–	ns
Tlo	Clock Low Time	15	–	ns

(1) As measured on Honeywell tester.

Power Up, Power Down and Power Interruption Sequencing

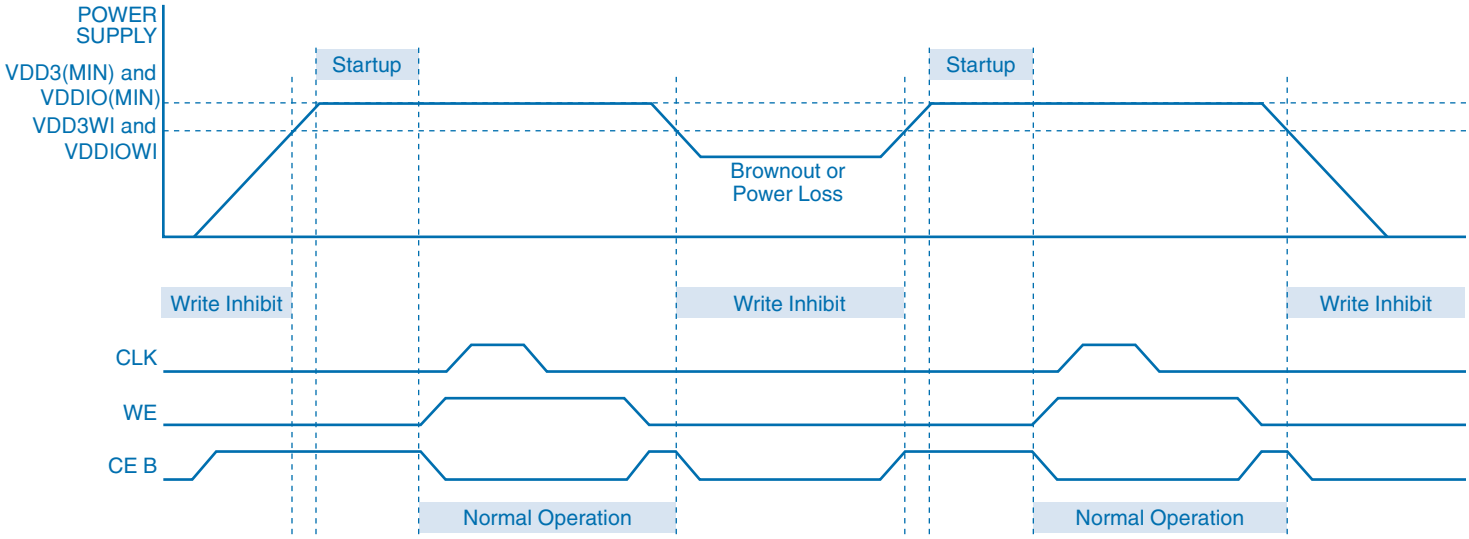
There are power sequencing requirements due to the on-chip voltage regulator and to protect against inadvertent write operations to the MRAM. The internal voltage regulator converts the VDD3 3.3V input power to 1.8V for the internal circuitry. On power up, as soon as VDD3 is equal to or exceeds VDD3(MIN) and VDDIO is equal to or exceeds VDDIO(MIN), there is a startup time of 2mS before read and write operations can start. This time allows memory power supplies to stabilize. The ramp rates on the VDD3 and VDDIO supply should not exceed 1 second in duration for either rising or falling.

During both power up and power down, care must be taken to ensure there are no inadvertent WRITE cycles started due to noise or glitches. It is required that the control signals CLK and WE pins be held low (VIL or lower) until after the 2mS startup is complete.

The MRAM is protected from write operations whenever VDD3 is less than VDD3WI which was designed for approximately 2.65V and whenever VDDIO is less than VDDIOWI which was designed for approximately 1.90V. During power loss or brownout where VDD3 goes below VDD3WI or VDDIO goes below VDDIOWI, writes are protected and a startup time must be observed when VDD3 returns equal to or greater than VDD3(MIN) and VDDIO returns equal to or greater than VDDIO(MIN).

Following a power-up condition; a no-op (dummy) read clock cycle with CE_B=low, auto_incr=low and WE=low must be performed to complete part initialization.

Power Sequencing Characteristics



Reliability

For many years Honeywell has been producing integrated circuits that meet the stringent reliability requirements of space and defense systems. Honeywell has delivered hundreds of thousands of QML parts since first becoming QML qualified in the early 1990's. Using this proven approach Honeywell will assure the reliability of the products manufactured with the SOI CMOS process technology. This approach includes adhering to Honeywell's Quality Management Plan for:

- Designing in reliability by establishing electrical rules based on wear out mechanism characterization performed on specially designed test structures (electromigration, TDDB, hot carriers, bias temperature instability, radiation)
- Utilizing a structured and controlled design process
- A statistically controlled wafer fabrication process with a continuous defect reduction process
- Individual wafer lot acceptance through process monitor testing (includes radiation testing)
- The use of characterized and qualified packages
- A thorough product testing program based on MIL-PRF-38535 and MIL-STD 883.

Screening and Conformance Inspection

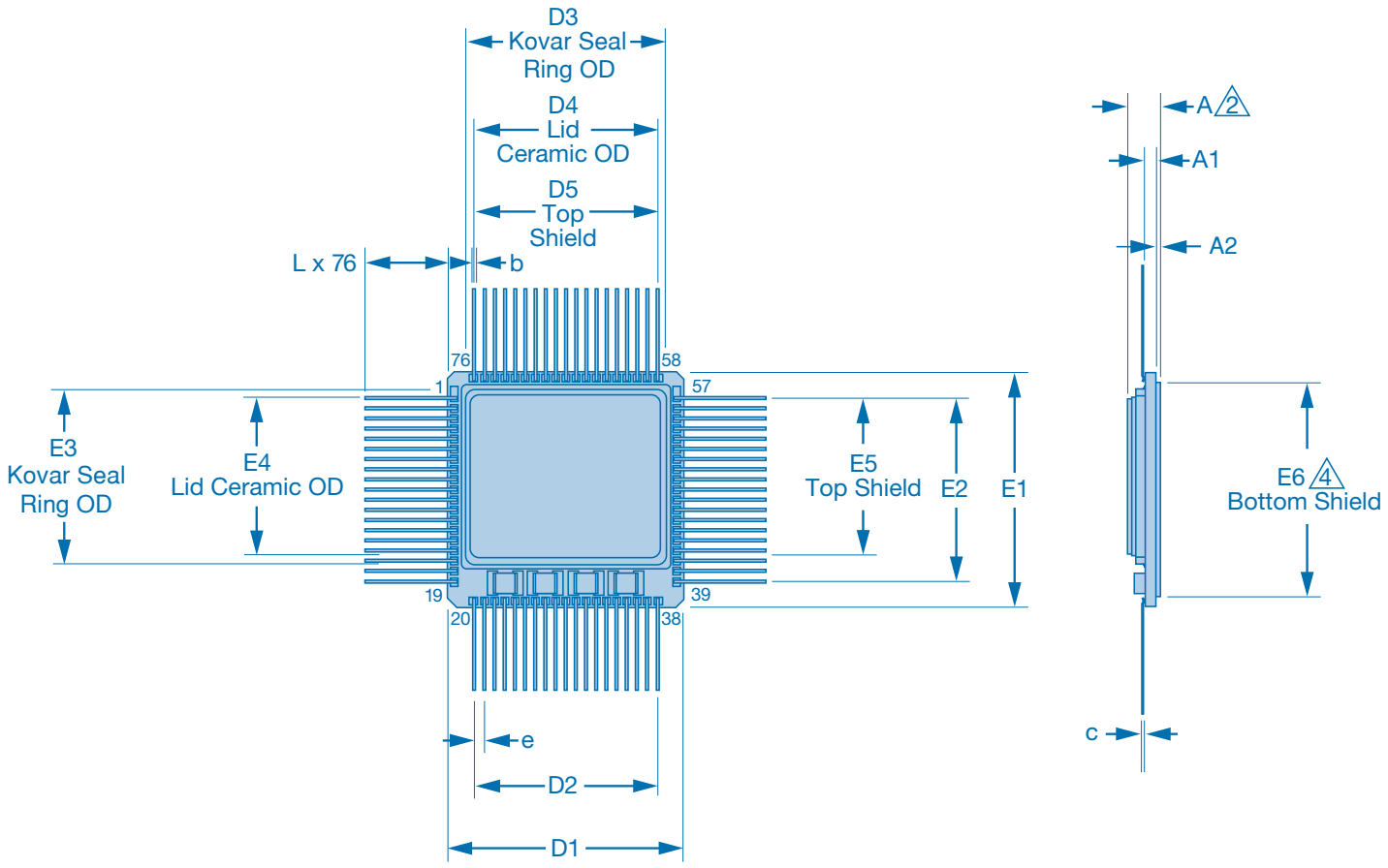
The product test flow includes screening units with the applicable flow (Engineering Model, QML V, QML Q, and the appropriate periodic or lot conformance testing (Groups A, B, C, D, and E). Both the wafer process and the products are subject to periodic or lot based Technology Conformance Inspection (TCI) and Quality Conformance Inspection (QCI) tests as defined by Honeywell's Quality Management Plan.

Conformance Test Summary

Group A	General Electrical Tests
Group B	Mechanical – Resistance to Solvents, Bond Strength, Die Shear, Solderability
Group C	Life Tests – 1000 hours at 125°C or equivalent
Group D	Package Related Mechanical Tests – Physical Dimensions, Lead Integrity, Thermal Shock, Temp Cycle, Moisture Resistance, Seal, Mechanical Shock, Vibration, Acceleration, Salt Atmosphere, Internal Water Vapor, Adhesion of Lead Finish
Group E	Radiation Tests

Package Outline

The 76 Lead Shielded Ceramic QFP Package (including external capacitors): Magnetic shielding is tied to ground on the package.



1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS.

2. A IS THE TOTAL THICKNESS OF THE TOP SHIELD, LID, SEAL RING, CERAMIC BODY, BOTTOM SHIELD, AND SHIELD ADHESIVES.

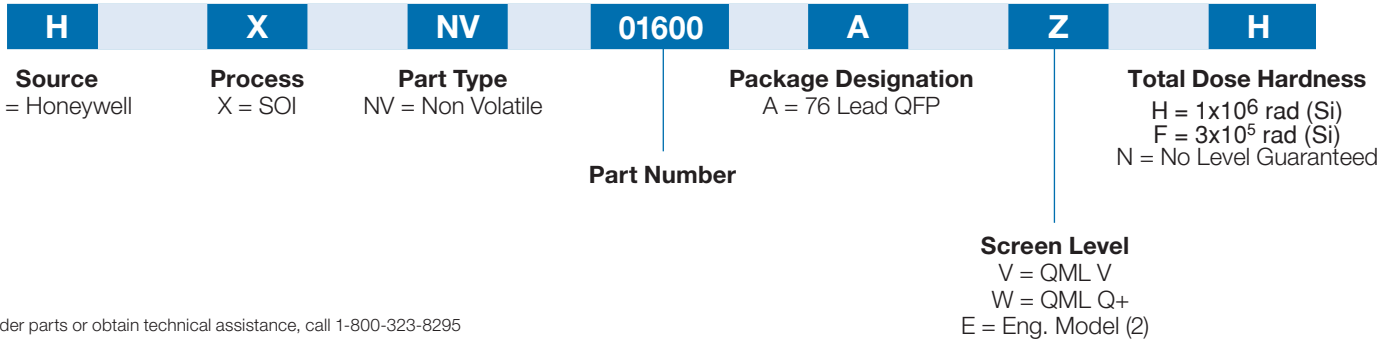
3. NOT APPLICABLE.

4. THE BOTTOM SHIELD IS SQUARE AND DIMENSION E6 REPRESENTS DIMENSIONS D6 AND E6.

	Common Dimensions Millimeters			Common Dimensions Inches		
Symbol	Min	Nom	Max	Min	Nom	Max
A	3.851	4.292	4.734	.152	.169	.186
A1	1.282	1.422	1.562	.050	.056	.062
A2	.559	.610	.660	.022	.024	.026
b	0.36	0.41	0.46	.014	.016	.018
c	0.10	0.15	0.20	.004	.006	.008
D1/ E1	28.91	29.21	29.51	1.138	1.150	1.162
D2/E2	–	22.86	–	–	.900	–
D3	24.895	25.095	25.295	.980	.988	.996
D4	22.711	22.911	23.111	.894	.902	.910
D5	22.581	22.708	22.835	.889	.894	.899
E3	21.670	21.870	22.070	.853	.861	.869
E4	19.485	19.685	19.885	.767	.775	.783
E5	19.355	19.482	19.609	.762	.767	.772
D6/E6	26.543	26.670	26.797	1.045	1.050	1.055
e	–	1.27	–	–	.050	–
L1	10.160	10.414	10.668	.400	.410	.420

Ordering Information (1)

QML qualified MRAM parts shall be ordered to the SMD 5962-13212. The SMD is the governing document and shall take precedence if there are conflicts with the datasheet.



(1) To order parts or obtain technical assistance, call 1-800-323-8295

(2) Engineering Model Description: Parameters are tested from -40°C to 125°C, 48-hour burn-in, no radiation guarantee.

QCI Testing (1)

Classification	QCI Testing
Q+	No lot specific testing performed. (2)
V	Lot specific testing required in accordance with MIL-PRF-38535 Appendix B.

(1) QCI groups, subgroups and sample sizes are defined in MIL-PRF38535 and the Honeywell QM Plan. Quarterly testing is done in accordance with the Honeywell QM Plan.
(2) If customer requires lot specific testing, the purchase order must indicate specific tests and sample sizes.

Find out more

To learn more about Honeywell's radiation hardened integrated circuit products and technologies, visit www.honeywellmicroelectronics.com.

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